L19 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:606806 HCAPLUS
DN 133:186522
TI Using NO or N2O treatment to generate **different** oxide **thicknesses** in one oxidation step for single poly nonvolatile memory fabrication
IN Yu, Mo-chiun; Chu, Wen-ting; **Jang, Syun-min**
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-8247
NCL 438258000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6110780	A	20000829	US 1999-283842	19990401

PRAI US 1999-283842 19990401

AB A new method of using a NO or N2O treatment on a 1st area on a wafer to form a thinner oxide film in the 1st area and a thicker oxide film in a 2nd area on a wafer using a single oxidn. step is achieved. A semiconductor substrate of a Si wafer is provided wherein a 1st area is sepd. from a 2nd area by an isolation region. The Si substrate in the 2nd area is treated with NO or N2O whereby a high-N Si oxide layer is formed on the surface of semiconductor substrate in the 2nd area. A tunnel window is defined in the 1st area and the oxide layer within the tunnel window is removed. The Si wafer is oxidized whereby a tunnel oxide layer forms within the tunnel window and whereby a gate oxide layer is formed overlying the high-N Si oxide layer in the 2nd area. The tunnel oxide layer has a greater thickness than the combined thickness of the gate oxide layer and the high-N Si oxide layer. A conducting layer is deposited and patterned overlying the tunnel oxide layer and the gate oxide layer and fabrication of the integrated circuit device is completed.
single poly nonvolatile memory fabrication)

IT 7631-86-9P, Silica, processes 11105-01-4P, Silicon nitride oxide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process); USES (Uses)
(using nitric oxide or nitrogen oxide treatment to generate **different** oxide **thicknesses** in one oxidn. step for single poly nonvolatile memory fabrication)

IT 10024-97-2, Nitrogen oxide (N2O), uses 10102-43-9, Nitric oxide, uses
RL: NUU (Other use, unclassified); RCT (Reactant); RACT (Reactant or reagent); USES (Uses)
(using nitric oxide or nitrogen oxide treatment to generate **different** oxide **thicknesses** in one oxidn. step for single poly nonvolatile memory fabrication)

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
RE
(1) Ajika; US 5600164 1997 HCAPLUS

L19 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:71767 HCAPLUS
DN 138:129800
TI Method for making FET gate oxides with **different thicknesses** using a thin silicon nitride layer and a single oxidation step
IN Yu, Mo-Chiun; **Jang, Syun-Ming**
PA Taiwan Semiconductor Manufacturing Computer, Taiwan
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-8234
NCL 438275000; 438221000; 438225000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6511887	B1	20030128	US 2000-596747	20000619
PRAI US 2000-596747		20000619		

AB The invention relates to a method for making a dual-gate oxide field effect transistor. The method utilizes a patterned thin silicon nitride layer and a single rapid thermal oxidn. step to form a thicker gate oxide for memory and peripheral circuits while forming a thin nitrogen rich gate oxide for high-performance logic circuits. After forming STI around the logic and memory call areas and removing any native oxide, a thin CVD silicon nitride layer is deposited. The Si3N4 is patterned to leave portions over the logic device areas. A single rapid thermal oxidn. process is performed to grow a thicker gate oxide on the exposed memory areas while concurrently the Si3N4 is slowly converted to a nitrogen-rich oxide and forms a thinner gate oxide on the logic device areas. The thinner nitrogen-rich gate oxide also retards boron diffusion to make more stable devices.
ST CMOS logic FET VLSI CVD CMP STI